CLAIMS

What is claimed is:

1. A high swing cascode biasing circuit, comprising:

first, second, third, fourth, fifth, and sixth transistors, each with a first terminal, a second terminal, and a control terminal,

wherein said second terminals of said first, third and fifth transistors communicate with said first terminals of said second, fourth and sixth transistors, said first terminal of said first transistor communicates with said control terminals of said third and fifth transistors, and said first terminal of said third transistor communicates with said control terminals of said fourth and sixth transistors;

a resistance having a first end that communicates with said first terminal of said first transistor and a second end that communicates with said control terminals of said first and second transistors;

a first capacitance having a first end that communicates with said control terminals of said first and second transistors and a second end that communicates with said second terminal of said fifth transistor and said first terminal of said sixth transistor; and

a second capacitance having a first end that communicates with said second terminal of said fifth transistor and said first terminal of said sixth transistor.

2. The high swing cascode biasing circuit of Claim 1 further comprising a third capacitance having a first end that communicates with said second terminal of said first transistor and a first terminal of said second transistor.

3. The high swing cascode biasing circuit of Claim 1 wherein the frequency boosting circuit is implemented in an Ahuja compensation circuit.

4. The high swing cascode biasing circuit of Claim 1 wherein said first, second, third, fourth, fifth, and sixth transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

5. The high swing cascode biasing circuit of Claim 1 wherein said resistance is one of a standard fixed-value resistor, a nonlinear variable resistor and a metal-oxide-semiconductor (MOS) resistor.

6. A high swing cascode biasing circuit, comprising:

a current biasing circuit including first, second, third and fourth transistors, wherein said second terminals of said first and third transistors communicate with said first terminals of said second and fourth transistors, said control terminal of said first transistor communicates with said control terminal of said second transistor, and said first terminal of said third transistor communicates with said control terminal of said fourth transistor;

a current mirror circuit that includes fifth and sixth transistors each including a control terminal and first and second terminals and a first capacitance having one end connected between said second terminal of said fifth transistor and said first terminal of said sixth transistor;

a resistance having one end that communicates with said first terminal of said first transistor and an opposite end that communicates with said control terminal of said first transistor; and

a second capacitance having one end that communicates with said control terminals of said first and second transistors and an opposite end that communicates with said one end of said first capacitance.

7. The high swing cascode biasing circuit of Claim 6 further comprising a third capacitance having one end that communicates with said second terminal of said first transistor and said first terminal of said first capacitance.

8. The high swing cascode biasing circuit of Claim 6 wherein the frequency boosting circuit is implemented in an Ahuja compensation circuit.

9. The high swing cascode biasing circuit of Claim 6 wherein said first, second, third and fourth transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

10. The high swing cascode biasing circuit of Claim 6 wherein said resistance is one of a standard fixed-value resistor, a nonlinear variable resistor and a metal-oxide-semiconductor (MOS) resistor.

11. A high swing cascode biasing circuit, comprising:

a current biasing circuit that generates a cascode bias and a main bias;

a frequency boosting circuit that receives said cascode bias and said main bias; and

a current mirror circuit that receives said main bias.

12. The high swing cascode biasing circuit of Claim 11 wherein said current mirror circuit includes a first transistor, a second transistor and a first capacitance having one end connected between said first and second transistors and wherein said frequency boosting circuit biases a control terminal of said first transistor and receives feedback from said one end of said first capacitance.

13. The high swing cascode biasing circuit of Claim 12 wherein said frequency boosting circuit comprises:

a third transistor that has a control terminal that receives said cascode bias, a first terminal and a second terminal; and

a fourth transistor that has a control terminal that receives said main bias, a first terminal that communicates with said second terminal of said third transistor and a second terminal.

14. The high swing cascode biasing circuit of Claim 13 wherein said frequency boosting circuit comprises a second capacitance having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said second terminal of said third transistor and with said one end of said first capacitance.

15. The high swing cascode biasing circuit of Claim 14 wherein said frequency boosting circuit comprises an inverter that has an input that communicates with said first terminal of said third transistor and an output that communicates with said control terminal of said first transistor.

16. The high swing cascode biasing circuit of Claim 15 wherein said frequency boosting circuit comprises a first resistance having one end that communicates with said input of said inverter and an opposite end that communicates with said output of said inverter.

17. The high swing cascode biasing circuit of Claim 12 wherein said first and second transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

18. The high swing cascode biasing circuit of Claim 12 wherein said feedback increases a transconductance of said first transistor.

19. The high swing cascode biasing circuit of Claim 11 wherein said frequency boosting circuit increases a bandwidth of said high swing cascode biasing circuit.

20. An Ahuja compensation circuit comprising the high swing cascode biasing circuit of Claim 11.

21. A high swing cascode biasing circuit, comprising:

current biasing means for generating a cascode bias and a main bias;

frequency boosting means for receiving said cascode bias and said main bias and for boosting a frequency response of said high swing cascode biasing circuit; and

current mirror means for receiving said main bias.

22. The high swing cascode biasing circuit of Claim 21 wherein said current mirror means includes a first transistor, a second transistor and first capacitance means for providing a first capacitance and having one end connected between said first and second transistors and wherein said frequency boosting means biases a control terminal of said first transistor and receives feedback from said one end of said first capacitance means.

23. The high swing cascode biasing circuit of Claim 22 wherein said frequency boosting means comprises:

a third transistor that has a control terminal that receives said cascode bias, a first terminal and a second terminal; and

a fourth transistor that has a control terminal that receives said main bias, a first terminal that communicates with said second terminal of said third transistor and a second terminal.

24. The high swing cascode biasing circuit of Claim 23 wherein said frequency boosting means comprises second capacitance means for providing a second capacitance and having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said second terminal of said third transistor and with said one end of said first capacitance means.

25. The high swing cascode biasing circuit of Claim 24 wherein said frequency boosting means comprises inverting means for inverting that has an input that communicates with said first terminal of said third transistor and an output that communicates with said control terminal of said first transistor.

26. The high swing cascode biasing circuit of Claim 25 wherein said frequency boosting means comprises first resistance means for providing a first resistance and having one end that communicates with said input of said inverter and an opposite end that communicates with said output of said inverter.

27. The high swing cascode biasing circuit of Claim 22 wherein said first and second transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

28. The high swing cascode biasing circuit of Claim 22 wherein said feedback increases a transconductance of said first transistor.

29. An Ahuja compensation circuit comprising the high swing cascode biasing circuit of Claim 21.